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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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•	Application No.	Applicant(s)	
	10/827,163	BENJAMIN ET AL.	
Office Action Summary	Examiner	Art Unit	
	Laura E. Martin	2853	
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address	
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	J. lely filed the mailing date of this communication. D (35 U.S.C. § 133).	
Status .			
Responsive to communication(s) filed on <u>02 Octoor</u> This action is FINAL . 2b) ☐ This Since this application is in condition for alloward closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro		
Disposition of Claims			
4) Claim(s) 1-103 is/are pending in the application 4a) Of the above claim(s) 1-21,29-31,34,35,37, 5) Claim(s) is/are allowed. 6) Claim(s) 22-28,32,33,36,39,42-44 and 96-101 7) Claim(s) 40 and 41 is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers 9) The specification is objected to by the Examine. 10) The drawing(s) filed on is/ are: a) access Applicant may not request that any objection to the oregenerated.	38,45-95,102 and 103 is/are with is/are rejected. r election requirement. r. epted or b) □ objected to by the the drawing(s) be held in abeyance. See	Examiner. e 37 CFR 1.85(a).	
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.	
Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the prior application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on No ed in this National Stage	
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Date of Informal F 6) Other:	ate	

DETAILED ACTION

Election/Restrictions

Newly submitted claims 102 and 103 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the independent claim is directed towards an address generator and a shift register, which is a differently structured fluid ejection device. This leads to a burdensome search.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 102 and 103 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22, 23, 28, 97, 100, and 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1) in view of Saunders et al. (US 5541629 A).

Cleland et al. disclose the following claim limitations:

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As per claim 22: a fluid ejection device comprising: a plurality of firing cells (figure 11A, figure 10, element 1001); a fire line electrically coupled to at least some of the firing cells (figure 10, elements PSn and 1001) adapted to receive from the controller (figure 2, element 215) an energy signal having energy pulses (figure 11A, element PS 1-8); and an address generator (figure 11A, element 18) configured to provide a series of address signals adapted to enable firing cells of the plurality of firing cells in a series of address timeslots, wherein the energy signal provides at least one energy pulse during each of the address timeslots in the series of address timeslots to energize selected enabled firing cells (column 17, lines 21-35).

As per claim 28: the address generator provides seven address signals as a set of address signals during each of the address timeslots in the series of address timeslots (figure 11A, elements PS 1-8).

As per claims 100 and 101: receiving in the fluid ejection device from a controller external to the fluid ejecting device (figure 2, element 215), an energy signal on a fire line electrically coupled to at least some of a plurality of firing cells in the fluid ejection device (figure 10, elements PSn and 1001), the energy signal having energy pulses (figure 11A, elements PS1-8), generating a series of address signals (figure 11A, element 18) adapted to enable firing cells of the plurality of firing cell sin a series of timeslots, wherein the energy signal provides at least one energy pulse during each of the address timeslots in the series of address timeslots to energize selected enabled firing cells (column 17, lines 21-35).

Cleland et al. do not disclose the following claim limitations:

As per claims 22, 100, and 101: an address generator in a fluid ejection device.

As per claim 23: the address generator is configured to provide the series of address signals in a first sequence of the series of address signals and a second sequence of the series of address signals.

As per claim 97: the address generator is configured to provide the series of address signals in response to receiving a control pulse from the controller.

Saunders et al. disclose the following claim limitations:

As per claims 22, 100, and 101: an address generator in a fluid ejection device (abstract).

As per claim 23: the address generator is configured to provide the series of address signals in a first sequence of the series of address signals and a second sequence of the series of address signals (column 4, line 47-column 5, line 4).

As per claim 97: the address generator is configured to provide the series of address signals in response to receiving a control pulse from the controller (claim 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. with the disclosure of Saunders et al. in order to increase the nozzle number without increasing interconnections and to minimize the number of interconnections per driver.

Claims 24-27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1) and Saunders et al. (US 5541629 A), and further in view of Takahashi (US 5621440 A).

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Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 22.

Cleland et al. as modified do not disclose the following claim limitations:

As per claim 24: first sequence of the series of address signals is the reverse of the second sequence of the series of address signals.

As per claim 25: the address generator comprises: memory elements configured to provide output signals; and logic configured to receive the output signals and provide the series of address signals in response to the output signals, wherein the logic is configured to provide the series of address signals in the first sequence in response to the memory elements providing the series in a first output sequence and the logic is configured to provide the series of address signals in the second sequence in response to the memory elements providing the output signals in a second output sequence.

As per claim 26: the address generator comprises: first memory elements configured to provide first output signals; second memory elements configured to provide second output signals; first logic configured to receive the first output signals and provide the series of address signals in the first sequence in response to the first output signals; and second logic configured to receive the second output signals and provide the series of address signals in the second sequence in response to the second output signals.

As per claim 27: the address generator comprises: memory elements configured to provide output signals; first logic configured to receive the output signals and provide the series of address signals in the first sequence in response to the output signals;

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and second logic configured to receive the output signals and provide the series of address signals in the second sequence in response to the output signals.

As per claim 32: the address generator comprises: a shift register configured to provide output signals during each of the address timeslots in the series of address timeslots; and logic configured to receive the output signals during each address timeslot in the series of address timeslots and provide address signals in the series of address signals during each of the address timeslots in the series of address timeslots in response to the received output signals.

Takahashi et al. as disclose the following claim limitations:

As per claim 24: first sequence of the series of address signals is the reverse of the second sequence of the series of address signals (claim 23).

As per claim 25: the address generator comprises: memory elements configured to provide output signals; and logic configured to receive the output signals and provide the series of address signals in response to the output signals, wherein the logic is configured to provide the series of address signals in the first sequence in response to the memory elements providing the series in a first output sequence and the logic is configured to provide the series of address signals in the second sequence in response to the memory elements providing the output signals in a second output sequence (column 5, lines 38-46).

As per claim 26: the address generator comprises: first memory elements configured to provide first output signals (figure 25, elements 313 and 314); second memory elements configured to provide second output signals; first logic configured to

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receive the first output signals and provide the series of address signals in the first sequence in response to the first output signals; and second logic configured to receive the second output signals and provide the series of address signals in the second sequence in response to the second output signals (column 5, lines 38-46).

As per claim 27: the address generator comprises: memory elements configured to provide output signals; first logic configured to receive the output signals and provide the series of address signals in the first sequence in response to the output signals; and second logic configured to receive the output signals and provide the series of address signals in the second sequence in response to the output signals (column 5, lines 38-46 and figure 25, elements 313 and 314).

As per claim 32: the address generator comprises: a shift register configured to provide output signals during each of the address timeslots in the series of address timeslots (figure 13, element 103); and logic configured to receive the output signals during each address timeslot in the series of address timeslots and provide address signals in the series of address signals during each of the address timeslots in the series of address timeslots in response to the received output signals (column 5, lines 38-46).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. as modified with the disclosure of Takahashi in order to obtain sharp and high quality images and to improve upon recording speed.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1), Saunders et al. (US 5541629 A), and Takahashi (US 5621440 A), and further in view of Gibson et al. (US 5757394 A).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 32.

Cleland et al. as modified do not disclose the following claim limitations:

The logic is configured to pull down low at least one of the address signal provided during each of the address timeslots in the series of address timeslots.

Gibson et al. disclose the following claim limitations:

The logic is configured to pull down low at least one of the address signal provided during each of the address timeslots in the series of address timeslots (column 3, line 33 - column 4, line 32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. as modified with the disclosure of Gibson et al. in order to more efficiently read printer electronics.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1), Saunders et al. (US 5541629 A), and Takahashi (US 5621440 A), and further in view of Nakajima et al. (US 6476839 B1).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 32.

Cleland et al. as modified do not disclose the following claim limitations:

Signal lines configured to receive a series of pulses wherein the logic is configured to receive three pulses in the series of pulses.

Nakajima et al. disclose the following claim limitations:

Signal lines configured to receive a series of pulses wherein the logic is configured to receive three pulses in the series of pulses (claim 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. as modified with the disclosure of Nakajima et al. in order to improve print quality.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1), Saunders et al. (US 5541629 A), and Takahashi (US 5621440 A), and further in view of Hayasaki (US 6036297 A).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 32.

Cleland et al. as modified do not disclose the following claim limitations:

Signal lines configured to receive a series of pulses, wherein the shift register comprises shift register cells configured to receive an input signal and pulses in the series of pulses and to store the input signal in response to the received pulses.

Hayasaki discloses the following claim limitations:

Signal lines configured to receive a series of pulses, wherein the shift register comprises shift register cells configured to receive an input signal and pulses in the

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series of pulses and to store the input signal in response to the received pulses (column 9, lines 13-37).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. as modified with the disclosure of Hayasaki in order to improve print quality.

Claims 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1), Saunders (US 5541629 A), Takahashi (US 5621440 A), and Hayasaki (US 6036297 A), and further in view of Arakawa et al. (US 6270180 B1).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 33.

Cleland et al. as modified do not disclose the following claim limitations:

As per claim 42: each of the shift register cells comprises a first stage and a second stage and the first stage is configured to receive direction signals and the input signal.

As per claim 43: each of the shift register cells comprises a first stage and a second stage and the first stage of one of the shift register cells is configured to receive a control signal as the input signal.

As per claim 44: each of the shift register cells comprises a first stage and a second stage and the first stage of two of the shift register cells is configured to receive a control signal as the input signal.

Arakawa et al. disclose the following claim limitations:

As per claim 42: each of the shift register cells comprises a first stage and a second stage and the first stage is configured to receive direction signals and the input signal (figure 2, Dat0-Dat2 and CLKIN).

As per claim 43: each of the shift register cells comprises a first stage and a second stage and the first stage of one of the shift register cells is configured to receive a control signal as the input signal (figure 2, Dat0-Dat2 and CLKIN).

As per claim 44: each of the shift register cells comprises a first stage and a second stage and the first stage of two of the shift register cells is configured to receive a control signal as the input signal (figure 2, Dat0-Dat2 and CLKIN).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Cleland et al. as modified with the disclosure of Arakawa et al. in order to improve the quality of the printer.

Claim 96 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1) and Saunders et al. (US 5541629 A), and further in view of Gibson et al. (US 6022094 A).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 22.

Cleland et al. as modified do not disclose the following claim limitations:

The address generator is configured to disable the series of address signals in response to receiving a control signal from the controller.

Gibson et al. disclose the following claim limitations:

The address generator is configured to disable the series of address signals in response to receiving a control signal from the controller [0007].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the printing fluid apparatus taught by Cleland et al. with the disclosure of Gibson et al. to create more storage area in the printer.

Claim 98 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1) and Saunders et al. (US 5541629 A), and further in view of Hung et al. (US 20030189608 A1).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 22.

Cleland et al. as modified do not disclose the following claim limitations:

The address generator is configured to disable the series of address signals in response to receiving a control signal from the controller.

Hung et al. disclose the following claim limitations:

The address generator is configured to disable the series of address signals in response to receiving a control signal from the controller [0007].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the printing fluid apparatus taught by Cleland et al. with the disclosure of Hung et al. because it is well known in the art that controllers can control different aspects of a printer.

Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cleland et al. (US 6491377 B1) and Saunders et al. (US 5541629 A), and further in view of Schloeman et al. (US 200200186265 A1).

Cleland et al. as modified disclose the following claim limitations:

The fluid ejection device of claim 22.

Cleland et al. as modified do not disclose the following claim limitations:

A first address generator configured to provide the series of signals to a first subgroup of firing cells and a second address generator configured to provide the series of address signals to a second subgroup of the firing cells.

Schloeman et al. disclose the following claim limitations:

A first address generator configured to provide the series of signals to a first subgroup of firing cells and a second address generator configured to provide the series of address signals to a second subgroup of the firing cells [0007]; [0009]; [0016].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Cleland et al. with the disclosure of Schloeman et al. in order to provide multiple printheads within one printing unit. This allows for a multiple color image. It is well known in the art that multiple printheads can be used in a printer, each having its own address generator.

Allowable Subject Matter

Claims 40 and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 22-28, 32, 33, 36, 39-44, and 96-101 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura E. Martin whose telephone number is (571) 272-2160. The examiner can normally be reached on Monday - Friday, 7:00 - 3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen D. Meier can be reached on (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Laura E. Martin

MANISH S. SHAH PRIMARY EXAMINER